

DELAY-LOCK-LOOP WITH IMPROVED ACCURACY AND RANGE

Abstract of the Disclosure

A Delay-Lock-Loop circuit and a method for producing a phase shift comprises a phase generator producing a first and second clock signal having a first and second rising edge, respectively, wherein a timing difference between the first and second rising edges is equal to a desired cycle time; a delay circuit operable to receive the first clock signal and to produce a delayed clock signal; and a latch element connected to the delay circuit, and operable to check whether the delayed clock signal is delayed by an amount equal to the desired cycle time; a plurality of serially connected binary-weighted inverters connected to the latch element, which are operable to adjust the delay of the delayed clock signal to be equal to the desired cycle time; and a phase-shifted delay circuit connected to the delay circuit, and operable to produce multiple degrees of phase shift of the delayed clock signal.

Figures